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APPLICATION NO.	I	TILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,954		12/01/2003	Ryosuke Usui	14225-035001/F1030610US00 3594	
26211	7590	12/13/2005		EXAMINER	
FISH & RI	CHARD	SON P.C.	BREWSTER, WILLIAM M		
P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022				ART UNIT	PAPER NUMBER
				2823	
				DATE MAILED: 12/13/2005	;

Please find below and/or attached an Office communication concerning this application or proceeding.

				A
		Application No.	Applicant(s)	
		10/724,954	USUI ET AL.	
	Office Action Summary	Examiner	Art Unit	
		William M. Brewster	2823	
	The MAILING DATE of this communication app	pears on the cover sheet	with the correspondence address	s
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPL' CHEVER IS LONGER, FROM THE MAILING DA SIN (6) MONTHS from the mailing date of this communication. Operiod for reply is specified above, the maximum statutory period or re to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUI 36(a). In no event, however, may will apply and will expire SIX (6) M , cause the application to become	NICATION. a reply be timely filed ONTHS from the mailing date of this commur ABANDONED (35 U.S.C. § 133).	
Status				
2a) <u></u>	Responsive to communication(s) filed on <u>27 O</u> This action is FINAL . 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final.	·	rits is
Dispositi	on of Claims			
5)□ 6)⊠ 7)□	Claim(s) 1-12 and 14 is/are pending in the app 4a) Of the above claim(s) is/are withdraw Claim(s) is/are allowed. Claim(s) 1-12 and 14 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/o	wn from consideration.		
Applicati	on Papers			
10)	The specification is objected to by the Examine The drawing(s) filed on is/are: a) accomposition accomposition and any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Example.	epted or b) objected to drawing(s) be held in abey tion is required if the drawi	rance. See 37 CFR 1.85(a). ng(s) is objected to. See 37 CFR 1.	' '
Priority u	ınder 35 U.S.C. § 119			
12) a)l	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document: 2. Certified copies of the priority document: 3. Copies of the certified copies of the priority document: application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in rity documents have bee u (PCT Rule 17.2(a)).	Application No en received in this National Stag	l e
	e of References Cited (PTO-892)		v Summary (PTO-413)	
3) 🔲 Infor	e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date		o(s)/Mail Date f Informal Patent Application (PTO-152))

U.S. Patent and Trademark Office PTOL-326 (Rev. 7-05) Application/Control Number: 10/724,954

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DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., US Patent No. 6,528,879 B2 in view of Dery et al., US Patent No. 6,074,895.

Sakamoto teaches limitations from claims 1, 2, a circuit device manufacturing method comprising: in fig. 16A,

forming separation grooves 101 in a conductive foil 100 from a top surface to form conductive patterns that are integrally connected at the bottom portion of the conductive foil, col. 18, lines 30-63;

in fig. 17, mounting a circuit element 105 onto one or more of the conductive patterns; and, in fig. 18, sealing with a resin layer 18 so as to cover the circuit element and fill the separation grooves, col. 19, line 39 - col. 20, line 3; and

in figs. 18-21A, wherein a rear surface of the conductive foil is eliminated until the resin laver is exposed at the rear surface of the conductive foil to electrically separate the respective conductive patterns, col. 20, lines 20-41;

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limitations from claim 11, the method of claim 1 or 2, in fig. 14, wherein the conductive foil 100 is formed of a metal having copper as the principal material, col. 17, line 66 - col. 18, line 8;

limitations from claim 12, the method of claim 1 or 2, in fig. 17, wherein the circuit element comprises a semiconductor element 105A, that is electrically connected to one or more of the conductive patterns via metal wires 106, col. 19, lines 39-62;

limitations from claim 14, the method of claim 1, in fig. 17, wherein the separation grooves 101 extend only partially through the conductive foil.

Sakamoto (879) does not teach a plasma irradiation, but Dery does. Dery teaches in fig. 1A, limitations from claim 1, wherein plasma is irradiated onto the top surface of the conductive structures, and wherein contaminants attached to side surfaces of the separation structures are removed by ions reflected by the side surfaces, col. 3, lines 21-34, wherein the plasma cloud 116 generates plasma ions emanating from all directions including ones to irradiate the side structures; limitations from claim 2, irradiating plasma onto the top surface of the conductive structures, including the circuit element, col. 3, lines 21-34; and

limitations from claim 3, the method of claim 1, wherein irradiation of the plasma is carried out prior to the step of mounting the circuit element, col. 3, lines 21-34; limitations from claim 4, the method of claim 1, wherein irradiation of the plasma is carried out subsequent to the step of mounting the circuit element, col. 3, lines

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21-34, wherein for claims 2-4, the cleaning of the conductive structures and the circuit elements are beneficial giving the practitioner the option to gain advantages of plasma irradiation before and after circuit element attachment; limitations from claim 5, the method of claim 1 or 2, in fig. 1A, wherein contaminants attached to the surfaces of the separation grooves are removed by the plasma, col. 3, lines 21-34;

limitations from claim 6, the method of claim 5, wherein the contaminants comprise organic or inorganic matter, inorganic, col. 3, lines 21-34; limitations from claim 7, the method of claim 1 or 2, wherein the surface of the separation grooves are roughened by the plasma irradiation, col. 3, lines 21-34; limitations from claim 8, the method of claim 1 or 2, wherein the surface of the separation grooves are oxidized by the plasma irradiation, col. 3, line 64 - col. 4, lines 9, wherein the oxidizing affects the conductive structures as well; limitations from claim 9, the method of claim 1 or 2, wherein the plasma irradiation is carried out using oxygen gas, col. 3, line 64 - col. 4, lines 9; limitations from claim 10, the method of claim 1 or 2, wherein the plasma irradiation is carried out using an inert gas: argon, col. 3, line 64 - col. 4, lines 9.

Dery gives motivation in col. 3, lines 21-34. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Dery's process with Sakamoto's invention would have been beneficial because it can enhance adhesion between the device surfaces and the encapsulant.

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Other Prior Art

Examiner notes with interest, Igarashi et al., US Patent No. 6,889,428 B2 could be a §102(e) reference with an unperfected filing date of the application.

Response to Arguments

Applicant's arguments with respect to claims 1-12, 14 have been considered but are most in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2 December 2005 william M. Brewster WB